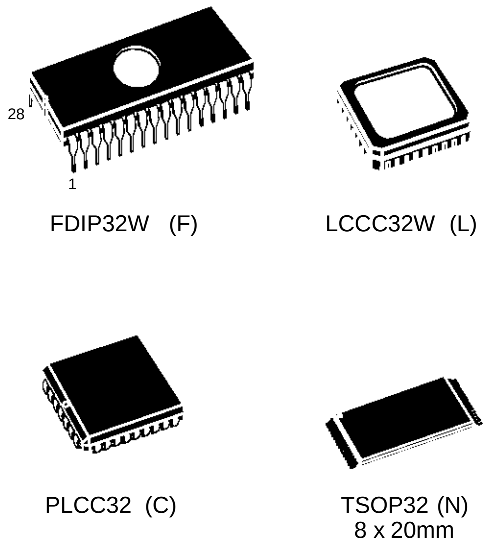
M27C2001

2 Megabit (256K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C2001 is a high speed 2 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C2001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Figure 1. Logic Diagram

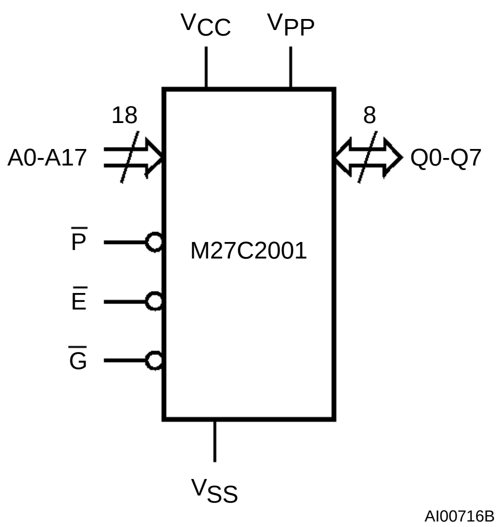


Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

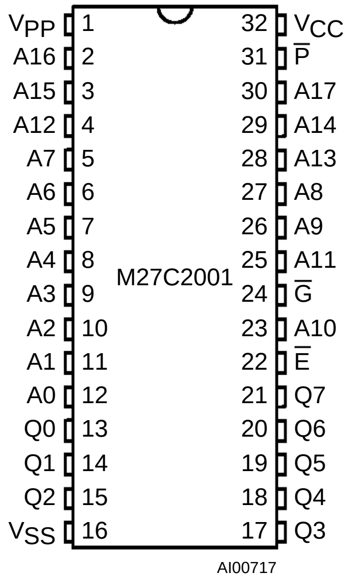


Figure 2B. LCC Pin Connections

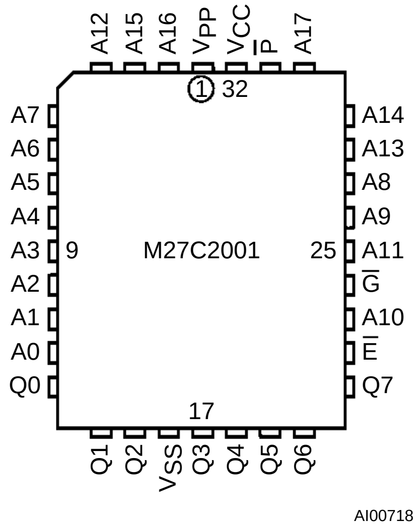
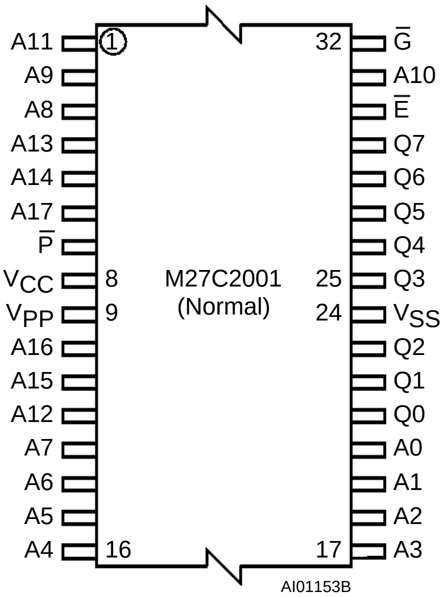


Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C2001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C2001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C2001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C2001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} [2]	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} [2]	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	1	0	0	0	0	1	61h

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

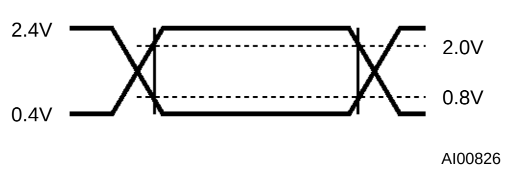


Figure 4. AC Testing Load Circuit

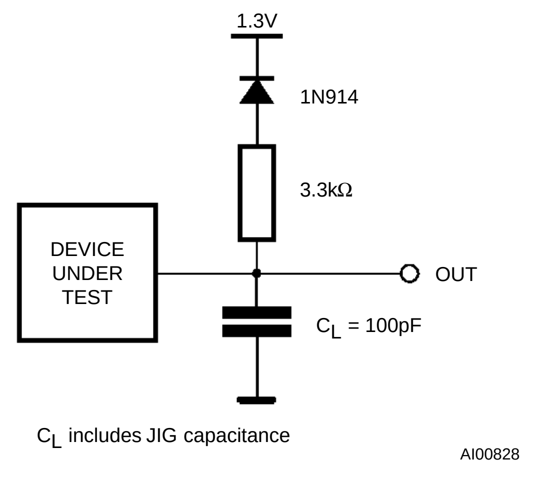


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C2001 -70 Min	-70 Max	-80 Min	-80 Max	-90 Min	-90 Max	Unit
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C2001 -10 Min	-10 Max	-12 Min	-12 Max	-15/-20/-25 Min	-15/-20/-25 Max	Unit
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

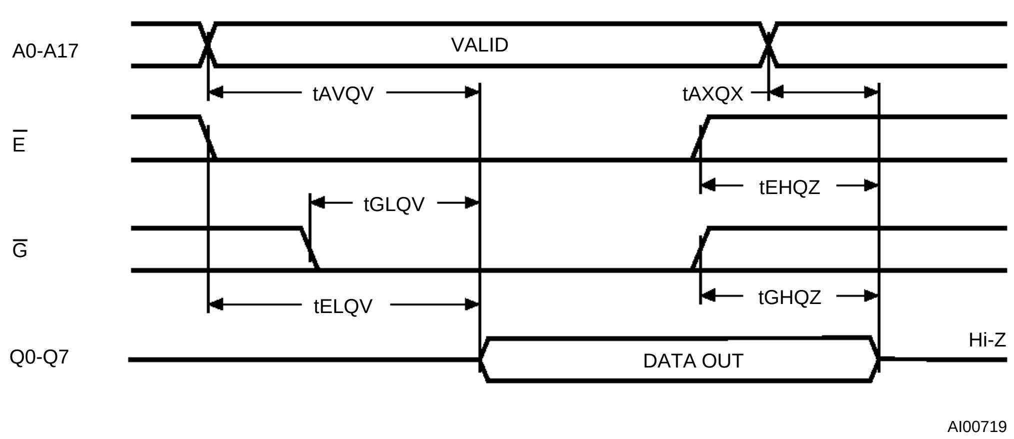


Table 8. Programming Mode DC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

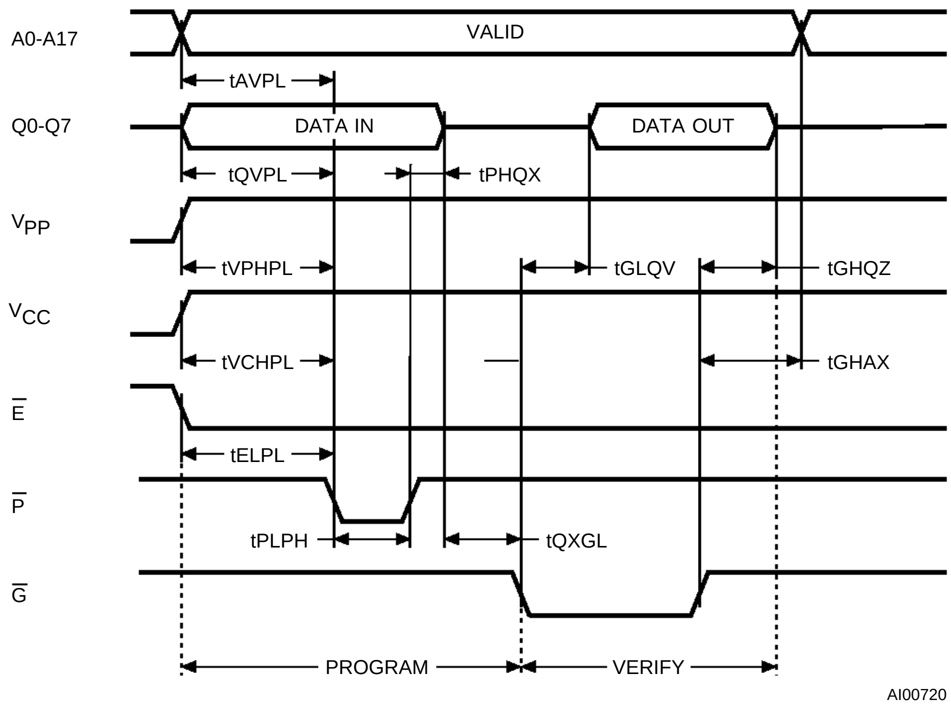
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} [2]	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



System Considerations

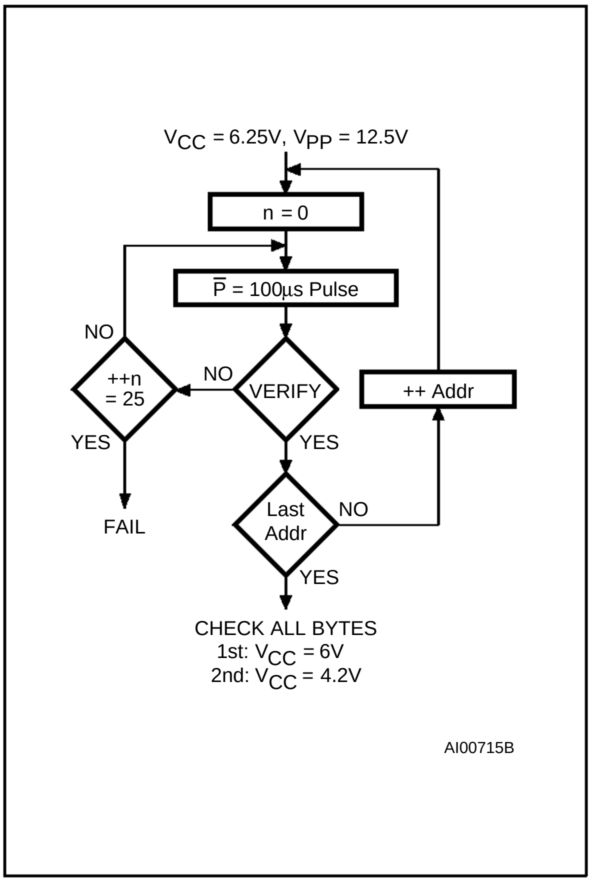
The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C2001 are in the ”1” state. Data is introduced by selectively programming ”0s” into the desired bit locations. Although only ”0s” will be programmed, both ”1s” and ”0s” can be present in the data word. The only way to change a ”0” to a ”1” is by die exposition to ultraviolet light (UV EPROM). The M27C2001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 26.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C2001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C2001 may be common. A TTL low level pulse applied to a M27C2001's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C2001. A high level $\overline{E}$ input inhibits the other M27C2001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C2001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C2001 with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C2001, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C2001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C2001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C2001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C2001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C2001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C2001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C2001 -80 X F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-70	70 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C	X	Additional Burn-in
-80	80 ns	blank	± 10%	L	LCCC32W	6	–40 to 85 °C	TR	Tape & Reel Packing
-90	90 ns			C	PLCC32				
-10	100 ns			N	TSOP32 8 x 20mm				
-12	120 ns								
-15	150 ns								
-20	200 ns								
-25	250 ns								

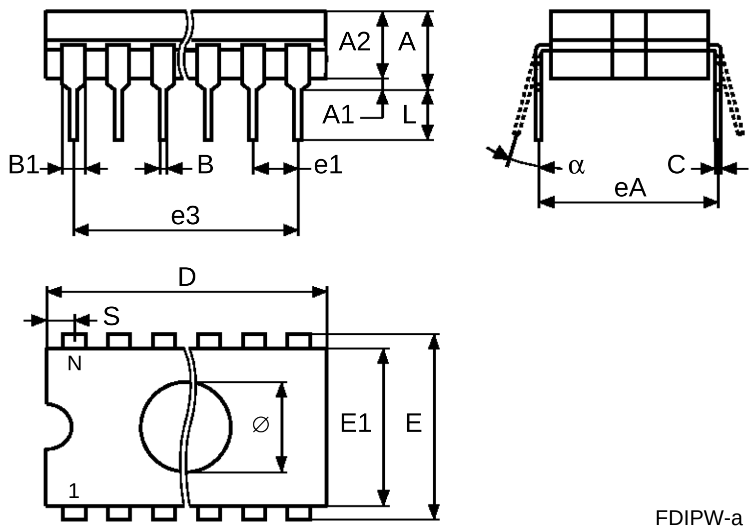
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP32W - 32 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			42.78			1.684
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	38.10	–	–	1.500	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	9.65	–	–	0.380	–	–
α		4°	15°		4°	15°
N	32			32		

FDIP32W



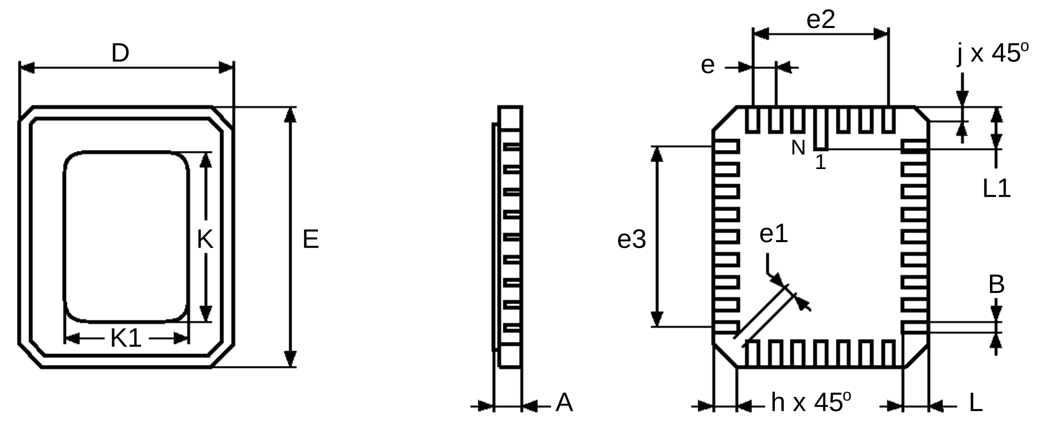
FDIPW-a

Drawing is not to scale

LCCC32W - 32 lead Leadless Ceramic Chip Carrier, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.28			0.090
B		0.51	0.71		0.020	0.028
D		11.23	11.63		0.442	0.458
E		13.72	14.22		0.540	0.560
e	1.27	–	–	0.050	–	–
e1		0.39	–		0.015	–
e2	7.62	–	–	0.300	–	–
e3	10.16	–	–	0.400	–	–
h	1.02	–	–	0.040	–	–
j	0.51	–	–	0.020	–	–
L		1.14	1.40		0.045	0.055
L1		1.96	2.36		0.077	0.093
K		10.50	10.80		0.413	0.425
K1		8.03	8.23		0.316	0.324
N	32			32		

LCCC32W



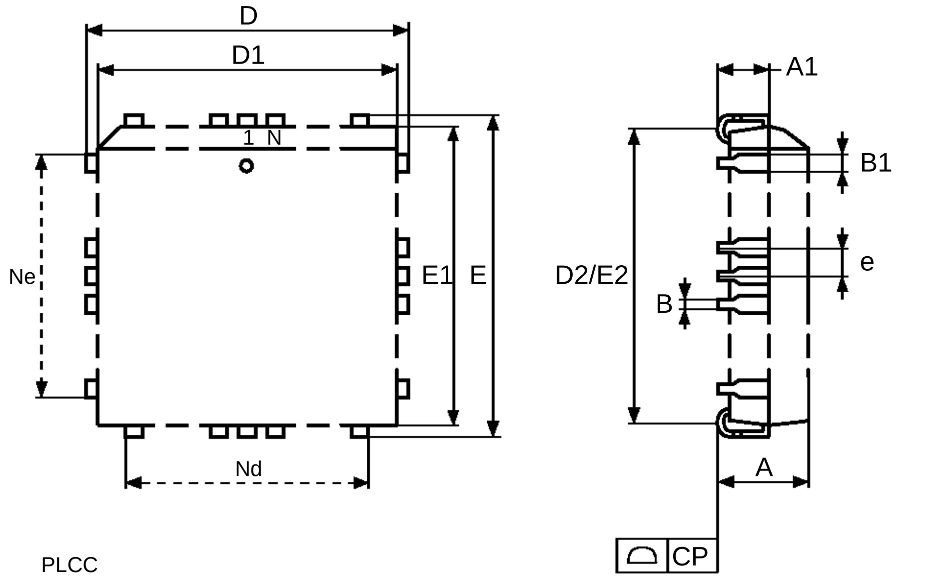
LCCCW-a

Drawing is not to scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32



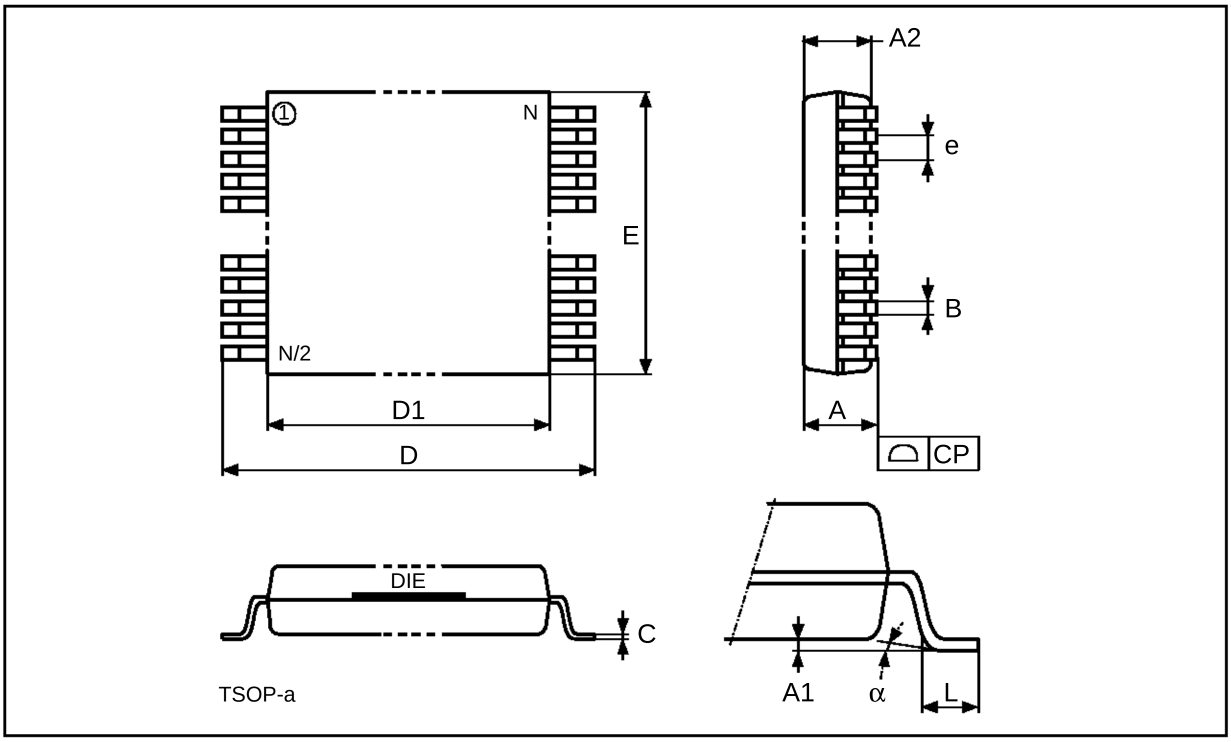
PLCC

Drawing is not to scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	**Min**	**Max**	**Typ**	**Min**	**Max**
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.004

TSOP32



Drawing is not to scale

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